

## **Remarks**

In the non-final June 28, 2006 Office Action, the Examiner rejected Claims 1-21 and objected to claim 1. By this Response, Applicants amend Claims 1-21 to clarify Applicants' claimed invention. No new matter is believed introduced by the clarifying amendments.

After entry of this Response, Claims 1-21 are pending in the Application. Applicants respectfully assert that Claims 1-21 are in condition for allowance and respectfully request reconsideration of the claims in light of the following remarks.

### **I. Pending Claims**

#### **Claim Rejection under 35 U.S.C. § 103(a)**

Claims 1-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ma et al. (U.S. Patent No. 6,075,741) in view of Applicants admitted prior art. Applicants respectfully traverse the rejection.

For an obviousness rejection to be proper, the Examiner must meet the burden of establishing a *prima facie* case of obviousness. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988).

For an obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970).

As amended, claim 1 recites, a system, comprising: a first write state machine; a second write state machine; a pulse generator operable to generate a first current draw waveform of current to the first write state machine and a second current draw waveform of current to the second write state machine; and a delay circuit operable to inject a time delay between the first current draw waveform and the second current draw waveform, and wherein the time delay is less than a duration of the current draw waveform applied to the first write state machine. Ma,

neither individually nor in view of the applicants admitted prior art, teaches nor suggests all of the elements of claim 1. More specifically, Ma does not teach or disclose inject a delay between the first current draw waveform and the second current draw waveform wherein the delay is less than a duration of the current draw waveform. Rather, Ma teaches inject a delay that is larger than the duration of the current draw waveform. In Column 6 lines 22 through 31 Ma states:

The delay produced by each delay stage, such as delay stages 42, 44, and 46 of staged delay circuit 40, must be sufficient to allow the Vbb voltage pump (not shown) circuit to sufficiently recover and thereby bring the substrate voltage Vbb away from the power supply Vcc voltage. A sufficient RC network delay in one embodiment of a 256 Mbit DRAM according to the present invention is approximately 10 microseconds which permits the Vbb voltage pump circuit to recover and sufficiently decrease the substrate voltage Vbb.

Therefore, the delay produced is substantially larger than the delay injected in the present invention. The system of Ma is a similar to a sequential programming system that is discussed in paragraph five of the present application. Accordingly, neither Ma nor the applicants teach or disclose all of the elements of claim 1.

Claims 8 and 15 disclose a method and a computer-readable medium that include delaying a second current draw waveform of current by a predetermined amount of time from a start of the first current draw waveform wherein the predetermined amount of time is less than a duration of the first current draw waveform. Ma, neither individually nor in view of the applicants admitted prior art, teaches nor suggests all of the elements of claims 8 and 15. More specifically, Ma does not teach or disclose that the predetermined amount of time is less than duration of the first current draw waveform. Rather, as explained above, Ma discloses a system similar to a sequential programming system as discussed in paragraph five of the present application, in which the predetermined amount of time is at least as long as the duration of the entire first current draw waveform. Accordingly, neither Ma nor the applicants teach or disclose all of the elements of claims 2 and 15.

Applicants, therefore, believe that Claims 1, 8, and 15 are allowable and that their respective dependent claims are also allowable for the further limitations contained therein. Accordingly, Applicants respectfully request withdrawal of all current rejections and issuance a Notice of Allowance in due course of patent office business.

## **II. Drawings**

Figures 1, 4, and 5 have been amended to correct errors in reference numerals.

Accordingly, please replace the first and third sheets of Figures with the attached Replacement Sheets.

## **III. Fees**

Applicants file this Response within three months of the June 28, 2006 Office Action and with no additional claims. Accordingly, Applicants believe that no extension or claims fees are due. The Commissioner is authorized, however, to charge any fees that may be required, or credit any overpayment, to Deposit Account No. 20-1507.

## **IV. Conclusion**

The foregoing is believed to be a complete response to the non-final Office Action mailed June 28, 2006. Applicants respectfully assert that 1-21 are in condition for allowance and respectfully request passing of this case in due course of patent office business. If the Examiner believes there are other issues that can be resolved by a telephone interview, or there are any informalities remaining in the application which may be corrected by an Examiner's amendment, a telephone call to Jeff Waters at (404) 885-3082 is respectfully requested.

Respectfully submitted,

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